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A Review on Carbon Nano Tubes Filed Effect Transistors in Different Era with Related Applications

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Abstract: Carbon nanotubes (CNTs) are solid potential substitutes for silicon in VLSI due to their remarkable abilities. We review the concept of operation of CNT - based FETs (CNFETs), the issues with respect to its cutting modern manufacture methods, execution parameters yielded by the most recent research; lastly, we show an outline of a few applications utilizing the special properties of these devices.

Key words: CNFET, CNT, CMOS

INTRODUCTION

Very-large-scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device. Before the introduction of VLSI technology most ICs had a limited set of functions they could perform. An electronic circuit might consist of a CPU, ROM, RAM and other glue logic. VLSI lets IC designers add all of these into one chip.

During the mid-1920s, several inventors attempted devices that were intended to control current in solid-state diodes and convert them into triodes. Success did not come until after WWII, during which the attempt to improve silicon and germanium crystals for use as radar detectors led to improvements in fabrication and in the understanding of quantum mechanical states of carriers in semiconductors. Then scientists who had been diverted to radar development returned to solid-state device development. With the invention of transistors at Bell Labs in 1947, the field of electronics shifted from vacuum tubes to solid-state devices. With the small transistor at their hands, electrical engineers of the 1950s saw the possibilities of constructing far more advanced circuits. As the complexity of circuits grew, problems arose

Carbon Nanotube Electronics

A carbon nanotube field-effect transistor (CNTFET) refers to a field-effect transistor that utilizes a single carbon nanotube or an array of carbon nanotubes as the channel material instead of bulk silicon in the traditional MOSFET structure. First demonstrated in 1998, there have been major developments in CNTFETs since Device operation was demonstrated at voltages below one volt. Characteristics obtained were comparable with conventional p-type MOSFETs. High normalized drive currents and transconductance values together with good subthreshold characteristics support the statement that carbon nanotubes are promising candidates for future device applications [1]. The output as well as the subthreshold characteristics can be understood within the framework of an SB carbon nanotube transistor.

The importance of the nanotube size for increased tunneling probability in the contact region and device performance as well as scaling behavior of SB-CNFETs are significantly being used in different from conventional MOSFETs.[2]-[4]

Nonidealities in CNFET

A circuit-compatible compact model for singlewalled CNFETs as an extension used to have non idealities in the device [5]. A universal model including the practical device nonidealities was implemented with HSPICE. More than one CNT per device was allowed, and the screening affected by the parallel channels can also include in the device model. Good agreement for both dc and ac characteristics between the device model and the experimental data can also be verified with the fabricated CNFET RF device. The S/D and SB resistances degrade the CNFET ON-current by a factor of two at the 32-nm node. Compared to silicon technology, the CNFET shows better device performance [based on the intrinsic CV/I gate-delay metric (six times for nFET and 14 times for pFET)] than the MOSFET device at the 32-nm node, even with device nonidealities. This large speed improvement is significantly degraded (degradation of approximately five times) by interconnect capacitance in a real circuit

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environment. Increasing the number of CNTs per device was the most effective way to improve the circuit speed. Compared to CMOS circuits, the CNFET circuits with one to ten CNTs per device was about two to ten times faster, the energy consumption per cycle is about seven to two times lower, and the EDP was about 15–20 times lower, considering the realistic layout pattern and the interconnect capacitance.

The complete CNFET device model is implemented hierarchically in three levels (Fig. 2). Device nonidealities are included hierarchically at each level. Level 1, is denoted as CNFET_L1, models the intrinsic behavior of MOSFET like
CNFET [6] [7]. The second level, denoted as CNFET_L2, includes the device nonidealities: the capacitance and resistance of the doped S/D CNT region, as well as the possible SB resistances of S/D contacts. The first two levels deal with only one CNT under the gate. The top level, denoted as CNFET_L3, models the interface between the CNFET device and the CNFET circuits. Further improvements to the implemented device model may include the following: 1) This model utilizes a simplified band structure which restricts the use of this model for the applications that require a high power supply and high CNT surface potential (_1.0 eV). A more complete band- structure model can alleviate this issue. Separating the operation region into multiple sections and deriving approximated analytical equations in each section are another ways to both enlarge the applicable range and improve the runtime.2) For a better subthreshold behavior modeling, the surface potential lowering and the consequent higher current caused by the holes (electrons) that pile up in the nFET (pFET) channel region should be considered, particularly in the high-bias region, [8] 3) the diffusion capacitance due to the minorcarriers at the S/D junctions, which may affect the ac response of small-signal analog circuits can also be defined according to the circuits. 4) One way to further improve CNFET circuit performance was to use metallic CNTs, multiwalled CNTs, or large- diameter CNTs as interconnects because of the much higher current density and much smaller parasitic fringe capacitance.[9]. 5) A more accurate device model should also include the defect and device reliability analysis. Most of the carrier scattering and thermal relaxation processes occur around the contact/junction region due to the nearballistic transport; thus, defects are likely to accumulate along the nanotubes, specifically around the contact region for shortgate CNFET.

Designing of OPAMP in CMOS and CNFET

The designing of opamp is quite easy but to deisgn a device using CMOS and CNFET is a big task. The advantages and disadvantages offered by newly emerging CNFET technology over the existing bulk CMOS which ceases to scale further to deliver the desired performance merits. Moreover, dependency on performance requirements, diameter (also responsible for scaling) plays an important role and will limit the performance delivered by CNFET in future e.g. low power design suits to smaller diameter while sacrificing the higher bandwidth requirements. Complex circuits could be investigated along with their hybrids and other nanoscale alternatives could also be taken up for performance comparison to explore their capabilities for future analog and mixed-signal designs along with some demonstrated fabrication experiments.

Designing of Metallic-Carbon-Nanotube-Tolerant Digital Logic Circuits

Metallic CNTs create source to drain shorts in CNFETs, resulting in undesirable effects such as excessive leakage, degraded noise margins, and delay variations. There was no known technique available at that time to grew 100% s-CNTs. Therefore, m-CNT removal techniques such as selective chemical etching are necessary. Unfortunately, such removal techniques were nonideal. Moreover, CNFET circuits exhibited statistical behaviour even with ideal m-CNT removal and the introduction of a probabilistic model which accounts for variations in CNT types (m- or s-), CNT diameters, and m-CNT removal processed significantly

Ternary Logic Gates and Arithmetic Circuits

The design of the new ternary logic family based on CNTFETs was given according to the need with the advancement in technology. As the threshold voltage of the CNTFET is function of the geometry of the CNTFET (i.e., the chirality), a novel multidiameter (multithreshold voltage) CNTFET-based ternary design had been acoordingly. A complete set of ternary gates can be implemented using multidiameter CNTFETs. A few ternary arithmetic circuits such as the HA and multiplier have been also designed to show the effectiveness of the proposed ternary family for circuit design. Compared with previous CNTFET-based designs, the proposed ternary gates achieved high performance, low power, and small area due to the removal of resistors and the utilization of binary gates in the design of arithmetic circuits[10]
The fundamental gates in the design of digital systems are the inverter, the NOR gate, and the NAND gate. [11]

Ultra Fast CNFET Comparator and CMOS Implementation Comparison

CNFET comparator and its key performances like rise and delay, gain, average power, transient responses from their simulation results by using HS pice model of CNFET. These results were compared with the simulations results of the comparator simulated in a 0.5µm CMOS

It could easily be concluded that for same DC biasing current, CNFET comparator shows much better performance with much faster output response, higher gain, lower average power dissipation and improved transient response with no spike in supply current like its CMOS counterpart. These promising findings make the CNFET comparator a better choice for future nano-electronic devices and circuits.[12]

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Low-Power Ultra wideband CCII
Ultra-wideband is a technology for transmitting information spread over a large bandwidth (>500 MHz); this should, in theory and under the right circumstances, be able to share spectrum with other users CNFET based dual output current conveyor at 32-nm technology can be made and nodding can also be done on the basis of optimum parameters of CNFET. The performance of CNFET-based CCII was further improved by optimizing parameters of individual CNFET giving rise to ITOPT. ITOPT provides excellent voltage and current bandwidths along with good port resistances, thus making it a viable proposition for ultrawideband systems. Next, the frequency characterization of the current conveyor is presented.

The frequency response of voltage gain between terminals Y and X of the current conveyor is analysed accordingly. It is to be noted that the static voltage gain close to unity was obtained.[13] The overall design and analysis clearly indicates that a CNFET can significantly achieve better performance than CMOS even at a scaled supply voltage of 0.7 V with the added advantage of lower power consumption.

Evaluation of CNFET Based Operational Amplifier Beyond 45-nm
Under this section the researchers has successfully investigated the important design metrics of CMOS- and CNFET-based op amp at 32- nm technology node. The overall design and performance analysis clearly indicated that the CNFET-based op amp has excellent performance in terms of AC gain, input impedance and output impedence.[14] Further improvements in gain-bandwidth product by scaling down the circuit to 22- nm node may be possible with optimized CNFET.

ZigBee using ±0.9V 32nm CNFET ICC-II
The researchers have explored the possibilities and design of analog integrated circuits using Carbon Nanotube FETs. The performance and analysis a of CNFET-based low-voltage lowpower ICC-II has been presented. Simulation tests confirm the correct operation of the proposed device for frequencies upto 5 GHz. A new voltage-mode universal filter employing the CNFET-based ICC-II was then discussed. HSPICE simulation results confirmed the applicability of the circuit to the entire ZigBee operating range. [15]

The proposed model shows the continuous-time analog filter capable of simultaneously performing the Low-Pass, Band-Pass and High-Pass functions. It employs two active elements, two grounded capacitors and three resistors (out of which two are grounded), which allow for ease of integration [15]
Further, optimization issues of power dissipation were explored in the context of nanotube count in the CNFETs. The presented filter could be a suitable candidate for replacing CMOS based electronics in the future.

Performance Comparison of a Current Conveyor in 0.35 µm & 65 nm CMOS and 32 nm CNFET A
comparative performances of 0.35µm and 65nmCMOS and 32nm CNFET – based inverting current conveyor additionally, the issues and challenges of CMOS downscaling like current tunneling effect is analysed, high power dissipation and short channedl effects etc. were discussed. HSPICE simulation was used to obtain the performance comparison test results which showed that 32nm CNFET based design outperforms its CMOS counterpart and works well for frequencies beyond 10GHz[16]. It leads to the conclusion that CNFET based designs could be siutable alternatives for the beyond-CMOS era. That would result in low voltage low power solutions for applications such as portable electronics and high frequency communications

CNFET based design of resilient MCML XOR/ XNOR circuit at 16nm technology node.
The authors have observed and computed design matrix like tp, PWR, PDP, and EDP, for CMOS and MCML based inverter and XOR circuits. It was found that MCML based circuits offer lower tp, PDP and EDP. This work also successfully investigates variability analysis of CMOS and MCML based XOR circuit in terms of PDP. MCML based logic styles ensure the best possible robustness in the face of variations. Further, the same is realized with CNFET technology. The proposed CNFET realization exhibits lower tp, PDP and EDP compared to its MOSFET counterpart.[17]

The significant fact that has given momentum to the use of CNFET is that, its device structure and operating principle are similar to that of CMOS that is why CNFET is known to be the best current carrying capability devise,
Later on the authors have proposed a circuit of CNFET based MCML XOR/ XNOR gate through which they have successfully investigated tp, PDP and EDP for MCML gate which is realized with CNFET

A Semi physical Large-Signal Compact Carbon Nanotube FET Model for Analog RF Applications
In this model, smooth current and charge formulations for semiconducting and metallic CNTs had been given, which are suitable for large-signal operation. A bipolar transport, temperature dependence with self-heating, noise, and a simple trap model have also been including. The physical meaning of the key model parameters allows, for a given gate length, geometry scaling from single-finger ST to multifinger MT ransistors. The new model, called CCAM shows an excellent agreement with DC as well as with bias and frequency dependent AC data of fabricated SB CNTFETs[18]. The model equations, especially those for tube charge, have also been verified based on ST FET simulations obtained from a solution of the BTE, including SB boundary conditions, and the Poisson equation. Implementation of the model equations in Verilog-A makes the model widely available across circuit simulators.

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Current-Mode High-Precision Full-Wave Rectifier Based on Carbon Nanotube Field Effect Transistors

A design of high precision rectifier circuit had been proposed and design consists of just four diode-tied carbon nanotube field effect transistors. The main attractive features of the proposed design are minimal number of transistors, small size, circuit simplicity, high accuracy and capability of rectifying signals with a relatively wide range of frequencies and amplitudes [19] FWR was proposed and performed the transient analysis for input signal amplitude 10μA.

Also the transient analysis of output waveforms was done with a frequency of 100 MHz and ultimately they did the DC characteristics as well. The performance of the rectifier was analyzed by evaluating the frequency dependent RMS error and DC transient value for different values of input current magnitudes.

The simulation results using HSPICE demonstrated that the -3db cutoff frequency for the input current magnitude of 0.1μA, 5μA, 10μA, 20μA, 50μA is about 9GHz, 140GHz, 190GHz, 326GHz and 427GHz, respectively. Simulation results of various temperatures (0°C–100°C) show that the proposed rectifier provides good temperature stability.[19]

Subthreshold leakage in CNFET & MOSFET @ 32-nm Technology Node

Comparative study of the MOSFETs and the CNFETs with respect to the subthreshold leakage current and the various factors affecting it such as, body effect, DIBL effect and temperature at 32-nm technology node analysed accordingly. A device is said to be biased in subthreshold region if the gate to source voltage is less than the threshold voltage. Ideally the device should be off in this region, but a drain to source current does not flow which is called subthreshold leakage current. [20]

Through their simulation and analysis it could be concluded that CNFETs have the potential to solve the problem of increased subthreshold leakage which is found in the silicon based devices below 45-nm technology node. They also have analyzed the impact of body effect and DIBL effect on the performance of both MOSFETs and CNFETs and found that CNFETs were much less sensitive to the short-channel effects as compared to MOSFETs. They also analyzed the impact of temperature variation on ION, IOFF and VTH and found that CNFET characteristics are much more resilient to temperature variations than that of MOSFETs.

Hence, superior leakage performance makes CNFET a very strong candidate to replace silicon based devices in future. However, in order for CNEFT to develop into a competitive technology the superiority of performance of CNFETs to MOSFETs has to be studied with respect to other matrices such as gate leakage current and band to band tunneling current

Low Power Consumption at Nano-scaled Era

In this paper the authors achieved very low power dissipation or consumption as compared to conventional CMOS. Also the power dissipation of various CNFET logic gates were calculated.

The authors also have discussed about the bandgap energy of CNT with various chiral vectors, CNFET based NOT, NAND, OR, X-OR and X NOR circuits were realized using a pulse input in order to get perfect results.[21] The conclusion resulted in this work was that the CNT based FET logic style was ideally suited to the deep submicron VLSI design technology for high performance systems.

CONCLUSION

In this paper we have discussed the summary of different paper related to CNFET. Also, we quickly talked about the structure of carbon nanotubes. We then introduced a review of some manufacture strategies, trailed by the issues most generally confronted amid these procedures.

An execution investigation highlighting essential operation ideas was displayed, and the outcomes of a few examination endeavors were researched. From this survey, it can be anticipated with a sensible level of certainty that CNT - based gadgets will be vital in the development of hardware sooner rather than later.

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